and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Feldmann in view of U.S. Pat. No. 6,075,770 to Chang et al. (hereinafter "Chang").

The Examiner has indicated that claims 2-4, 6-8, 12, 14-17, 21 and 24-26 would be allowable if rewritten in independent form.

In this response, Applicants traverse the §102(e) and §103(a) rejections. Applicants respectfully request reconsideration of the present application in view of the following remarks.

With respect to the §102(e) rejection of claims 1 and 5, Applicants respectfully submit that the Examiner has failed to establish that the Heijningen is prior art relative to the present application under §102(e). Applicants note that a §102(e) rejection requires that the invention was described in an "application for patent" or "patent granted." Since Heijningen is a publication in a journal, it does not meet these limitations. Nonetheless, with the goal of moving the application process forward, Applicants will continue to address the issue of whether Heijningen anticipates claims 1 and 5.

With respect to anticipation under §102, Applicants generally note that the Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §2131, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Independent claims 1 and 5 each comprise elements wherein the performance of an integrated circuit having an analog unit, a digital unit, and a substrate on which the units are located is simulated using "a lumped circuit in which the source [representing noise characteristics of the digital unit] couples to a lumped element representing the substrate and the substrate couples to a lumped element representing the analog unit." These claims, therefore, describe a model for carrying out simulations comprising "lumped" elements. For example, as part of the model, a lumped element representing an analog unit may be coupled to a lumped element representing the substrate in order to determine the effect of noise emitted by one or more digital circuits on one or more

analog circuits in a mixed analog and digital integrated circuit. See the Specification, p. 2, lines 27-31; p. 3, lines 23-25; p. 6, lines 4-9; and FIG. 2, element 204.

The Examiner, in formulating the §102 rejection, argues that each and every element of claims 1 and 5 is met by Heijningen. More specifically, the Examiner argues that the model comprising a substrate coupled to a lumped element representing an analog unit is described in Heijningen Sect. IV(a), 2nd Paragraph (Office Action, p. 4). Applicants respectfully disagree. Heijningen uses a model for simulating substrate noise comprising three mechanisms: coupling from digital power supply, coupling from switching source-drain nodes, and impact ionization in a MOSFET channel (Heijningen, Sec. III, 2nd Paragraph). Unlike claims 1 and 5, Heijningen does not describe a model comprising a lumped element representing an analog unit coupled to a substrate. Moreover, Heijningen, Sect. IV(a), 2nd Paragraph comes from a subsection entitled: "Substrate Noise Measurement Techniques." It states:

> A continuous-time direct measurement technique is the use of an analog differential amplifier, with one input connected to the substrate and the other to quiet reference signal [14], [15]. The sensor presented in [14], however, has only a limited bandwidth, and measurement of actual coupling from switching digital nodes is not possible due to this bandwidth limitation. A method for accurate measurement of the substrate noise up to 1 GHz, as presented in [15], is analyzed in more detail below.

This paragraph describes tangible analog circuitry to be used for measuring the electromagnetic noise produced by existing digital circuits. Heijningen uses these types of measurement devices to physically verify his simulations of substrate noise (Heijningen, Sec. I, 3rd Paragraph, and Sec. IV, 1st Paragraph). One skilled in the art will immediately recognize that this portion of the reference describes a technique for physically measuring existing devices as opposed to a technique for simulating devices in the manner claimed.

Based on these differences, Applicants respectfully submit that all the elements of claims 1 and 5 are not described by Heijningen, and that the claims should, therefore, be allowed.

With respect to the remaining §102(e) and §103(a) rejections, Applicants note that 37 C.F.R. §1.104(c)(2) requires that, in rejecting claims for want of novelty or for obviousness, "[w]hen a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable." Applicants further note that MPEP §7.06.02(i) states that, when making a rejection, "the particular part of a reference relied upon to support the rejection should be identified."

With respect to the §102(e) rejection of claim 9, Applicants note that claim 9 describes:

> A method comprising:
> identifying a candidate integrated circuit that comprises a candidate digital circuit;
> . . .
> fabricating said candidate integrated circuit when said power spectral density, $S(\omega)$, of said candidate digital circuit achieves a design goal for said candidate integrated circuit.

In formulating the §102(e) rejection, the Examiner argues that Feldmann anticipates all the limitations of this claim. However, the Examiner at least fails to expressly identify in the rejection where Feldmann anticipates the element of the claim beginning with "fabricating," as required by the Federal Rules and the MPEP. Applicants submit that, in fact, Feldmann contains no such description and therefore fails as a reference to describe each and every element in claim 9. Claim 9 should, therefore, be allowed over the Feldmann reference.

Applicants observe that claim 9 is also rejected under §103(a) as being unpatentable over Feldmann in view of Chang. The §103(a) rejection of this claim appears to be an error since this rejection discusses limitations not actually present in the claim. See the Office Action, p. 4. Applicants continue under this assumption.

With respect to the §103(a) rejection of independent claim 18 as unpatentable over Feldmann in view of Chang, Applicants submit that the Examiner again fails to specify what parts of Feldmann or Chang are relied upon to reject the element of the claim comprising "fabricating said candidate integrated circuit when said power spectral density, $S(\omega)$, of said candidate integrated circuit achieves a design goal for said candidate integrated circuit." Applicants submit that the references, in fact, contain no such description or suggestion. Therefore, the subject matter as a whole of claim

18 would not have been obvious at the time the invention was made, and the claim should be allowed.

With respect to the §103(a) rejection of claims 10, 19 and 23 as unpatentable over Feldmann in view of Chang, Applicants respectfully submit that Chang fails to supplement the above-described fundamental deficiencies of Feldmann as applied to independent claims 9 and 18. Therefore, the subject matter as a whole of dependent claims 10, 19 and 23 would not have been obvious at the time the invention was made and the claims should be allowed.

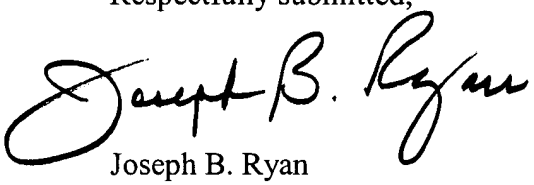
With respect to the §103(a) rejection of claims 11, 13, 20 and 22, Applicants note that in the Office Action, the Examiner only states the following:

> In view of claims 11, 13, 20 and 22, Feldmann et al. discloses an (*sic*) both digital and analog circuits (Col. 4 lines 15-40).
> (Office Action, p. 4).

Applicants submit that this rejection is substantially incomplete under MPEP 706.02(j), which specifies the proper content of a §103(a) rejection. Applicants continue to believe that claims 11, 13, 20 and 22 contain separately patentable matter and are in condition for allowance.

In view of the above, Applicants believe that claims 1-26 are in condition for allowance, and respectfully request the withdrawal of the §102(e) and §103(a) rejections.

Respectfully submitted,



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